I CLAIM:

1. A line-inversion LCD display driver, comprising:

a source driver suitable for switching one of a plurality of drive voltages to a column of LCD pixels in response to a digital code word, the transparency of each
5   of said pixels varying over a predetermined pixel voltage range, each of said pixels receiving said selected drive voltage at its first terminal and alternately switched between first and second voltages at its second terminal, said source driver comprising a plurality of resistors
10   connected in series and having accessible connection points at each end of said series string and at various resistor-resistor junctions along said series string, said series string producing at least some of said drive voltages when said connection points are connected to respective
15   correction voltages, and

a grayscale reference generator circuit, comprising:

a plurality of voltage sources, each of which is arranged to output a respective correction
20   voltage,

an interface circuit interposed between said voltage sources and said connection points, comprising:

a plurality of amplifiers, each of said amplifiers comprising:
25   an input which is coupled to first and second ones of said correction voltages, said first correction voltage closer to said negative supply rail than said positive supply rail and said second correction voltage closer to said positive supply rail than said
30   negative supply rail,

positive   and   negative   supply

rails,

a p-type differential transistor pair,

35 a first switchable current source connected to supply tail current to said p-type differential pair when enabled in response to a first control signal, said p-type differential pair connected to provide a first differential output current when said tail
40 current is supplied which varies with a differential input signal applied to said p-type pair's control inputs,

an n-type differential transistor pair,

a second switchable tail current
45 source connected to supply tail current to said n-type differential pair when enabled in response to a second control signal, said n-type differential pair connected to provide a second differential output current when said tail current is supplied which varies with a differential input
50 signal applied to said n-type pair's control inputs,

an output stage which receives said first and second differential output currents and is arranged to produce an output voltage at an output terminal which varies with said first and second differential output
55 currents, said output terminal being said amplifier's output, and

a control circuit which provides said first and second control signals such that said first switchable current source is enabled and said second
60 switchable current source is disabled when said first correction voltage is to be coupled to one of said connection points, and said second switchable current source is enabled and said first switchable current source is disabled when said second correction voltage is to be
65 coupled to one of said connection points.

2. The LCD display driver of claim 1, further comprising a plurality of two-to-one multiplexers, each of which is connected at its inputs to respective ones of said first and second correction voltages and which provides one

5 or the other of said first and second correction voltages at its output in response to said control signals, the control inputs of one transistor from each differential pair connected to a respective one of said analog mux outputs, said control circuit arranged to operate said mux

10 and said switchable current sources such that said first and second correction voltages are alternately connected to said connection points in synchronization with the switching of said pixels' second terminal such that the polarity of the voltages across said pixels is periodically

15 reversed.

3. The LCD display driver of claim 1, wherein the control inputs of one transistor from each differential pair are connected to respective ones of said first and second correction voltages, said control circuit arranged

5 to operate said switchable current sources such that said first and second correction voltages are alternately connected to said connection points in synchronization with the switching of said pixels' second terminal such that the polarity of the voltages across said pixels is periodically

10 reversed.

4. A rail-to-rail amplifier suitable for use in a line-inversion LCD grayscale reference generator circuit, comprising:

  positive and negative supply rails,

5   positive and negative input terminals,

  a p-type differential transistor pair,

  a first switchable current source connected to

supply tail current to said p-type differential pair when enabled in response to a first control signal, said p-type differential pair connected to provide a first differential output current when said tail current is supplied which varies with a differential input signal applied to said positive and negative input terminals,

an n-type differential transistor pair,

a second switchable tail current source connected to supply tail current to said n-type differential pair when enabled in response to a second control signal, said n-type differential pair connected to provide a second differential output current when said tail current is supplied which varies with a differential input signal applied to said positive and negative input terminals,

an output stage which receives said first and second differential output currents and is arranged to produce an output voltage at an output terminal which varies with said first and second differential output currents, said output terminal being said amplifier's output, said output voltage coupled back to said negative input terminal, said positive input terminal being said amplifier's input, and

a control circuit which provides said first and second control signals such that said first switchable current source is enabled and said second switchable current source is disabled when a voltage applied to said amplifier's input is closer to said negative supply rail than said positive supply rail, and said second switchable current source is enabled and said first switchable current source is disabled when the voltage applied to said amplifier's input is closer to said positive supply rail than said negative supply rail.

5.   The amplifier of claim 4, wherein said output

voltage is directly connected to said negative input terminal such that said amplifier operates as a unity gain buffer amplifier.

6. The amplifier of claim 4, wherein said output voltage is connected to said negative input terminal via a gain network such that said amplifier provides a gain other than one.

7. The amplifier of claim 4, wherein said p-type differential pair are PMOS field-effect transistors (FETs) having their sources connected to said first switchable current source, their gates connected to said positive and
5   negative input terminals, and their drains connected to said output stage, and said n-type differential pair are NMOS FETs having their sources connected to said second switchable current source, their gates connected to said positive and negative input terminals, and their drains
10   connected to said output stage.

8. The amplifier of claim 4, further comprising a multiplexer arranged to provide a first voltage to said amplifier's input when said first switchable current source is enabled and a second voltage to said amplifier's input
5   when said second switchable current source is enabled.

9. The amplifier of claim 4, wherein said p-type pair and said n-type pair each have an associated transconductance value of approximately g_m, said output stage including a compensation network which limits the
5   maximum amplifier bandwidth to avoid oscillation based on said transconductance value g_m.

10. The amplifier of claim 9, wherein said output

stage includes a folded cascode gain stage and a rail-to-rail output stage,

said rail-to-rail output stage comprising first 5 and second complementary transistors connected to conduct respective currents to a common output node in response to first and second voltages applied to their respective control inputs,

said folded cascode gain stage arranged to 10 receive said differential output currents and provide said first and second voltages to said first and second complementary transistors,

said compensation network comprising a first capacitor connected between the control input of said first 15 complementary transistor and said common output node, and a second capacitor connected between the control input of said second complementary transistor and said common output node.

11. The amplifier of claim 4, wherein each of said switchable tail current sources comprise:

a bias voltage,

a current source transistor which conducts said 5 tail current when biased with a bias voltage, and

a switching transistor which couples said bias voltage to said current source in response to said first control signal.

12. A line-inversion LCD display driver, comprising:

a source driver suitable for switching one of a plurality of drive voltages to a column of LCD pixels in response to a digital code word, the transparency of each 5 of said pixels varying over a predetermined pixel voltage range, each of said pixels receiving said selected drive voltage at its first terminal and alternately switched

between first and second voltages at its second terminal, said source driver comprising a plurality of resistors 10 connected in series and having accessible connection points at each end of said series string and at various resistor-resistor junctions along said series string, said series string producing at least some of said drive voltages when said connection points are connected to respective 15 correction voltages, and

a grayscale reference generator circuit, comprising:

a plurality of voltage sources, each of which is arranged to output a respective correction 20 voltage,

an analog multiplexer connected between said voltage sources and said resistor connection points and arranged to connect said correction voltages to respective connection points such that said series string produces a 25 desired array of drive voltages, said analog multiplexer arranged to switch the correction voltages connected to said connection points in synchronization with the switching of said pixels' second terminal such that the polarity of the voltages across said pixels is periodically 30 reversed, and

a plurality of amplifiers interposed between said analog multiplexer and said resistor connection points, each of said amplifiers comprising:

positive and negative supply rails,
35 positive and negative input terminals,
a p-type differential transistor pair,
a first switchable current source connected to supply tail current to said p-type differential pair when enabled in response to a first 40 control signal, said p-type differential pair connected to provide a first differential output current when said tail

current is supplied which varies with a differential input signal applied to said positive and negative input terminals,

45   an n-type differential transistor pair,

a second switchable tail current source connected to supply tail current to said n-type differential pair when enabled in response to a second control signal, said n-type differential pair connected to

50 provide a second differential output current when said tail current is supplied which varies with a differential input signal applied to said positive and negative input terminals,

an output stage which receives said

55 first and second differential output currents and is arranged to produce an output voltage at an output terminal which varies with said first and second differential output currents, said output terminal being said amplifier's output, said output voltage coupled back to said negative

60 input terminal, said positive input terminal being said amplifier's input, and

a control circuit which provides said first and second control signals such that said first switchable current source is enabled and said second

65 switchable current source is disabled when the voltage applied to said amplifier's input is closer to said negative supply rail than said positive supply rail, and said second switchable current source is enabled and said first switchable current source is disabled when the

70 voltage applied to said amplifier's input is closer to said positive supply rail than said negative supply rail,

each of said amplifier inputs connected to a respective one of the switched correction voltages from said analog multiplexer and each of said amplifier outputs

75 connected to a respective one of resistor connection

points.

13. A rail-to-rail amplifier suitable for use in a line-inversion LCD grayscale reference generator circuit, comprising:

positive and negative supply rails,

5   first and second voltages, said first voltage closer to said negative supply rail than said positive supply rail, and said second voltage closer to said positive supply rail than said negative supply rail,

first and second p-type transistors having 10 respective control inputs, said first p-type transistor's control input connected to said first voltage,

a first switchable current source connected to supply tail current to said p-type transistors when enabled in response to a first control signal, said p-type 15 transistors connected to provide a first differential output current when said tail current is supplied which varies with a differential input signal applied to said p-type transistors' control inputs,

first and second n-type transistors having 20 respective control inputs, said first n-type transistor's control input connected to said second voltage,

a second switchable tail current source connected to supply tail current to said n-type transistors when enabled in response to a second control signal, said n-type 25 transistors connected to provide a second differential output current when said tail current is supplied which varies with a differential input signal applied to said n-type transistors' control inputs,

an output stage which receives said first and 30 second differential output currents and is arranged to produce an output voltage at an output terminal which varies with said first and second differential output

currents, said output terminal being said amplifier's
output, said output voltage coupled back to said second
35 control inputs, and

a control circuit which provides said first and
second control signals such that said first switchable
current source is enabled and said second switchable
current source is disabled when said first voltage is to be
40 amplified by said amplifier, and said second switchable
current source is enabled and said first switchable current
source is disabled when said second voltage is to be
amplified by said amplifier.

14. The amplifier of claim 13, wherein said output
voltage is directly connected to said second control inputs
such that said amplifier operates as a unity gain buffer
amplifier.

15. The amplifier of claim 13, wherein said output
voltage is connected to said second control inputs via a
gain network such that said amplifier provides a gain other
than one.

16. The amplifier of claim 13, wherein said first and
second p-type transistors are PMOS field-effect transistors
(FETs) having their sources connected to said first
switchable current source, their gates connected to said
5 first voltage and said output terminal, respectively, and
their drains connected to said output stage, and said first
and second n-type transistors are NMOS FETs having their
sources connected to said second switchable current source,
their gates connected to said second voltage and said
10 output terminal, and their drains connected to said output
stage.

17. The amplifier of claim 13, wherein said p-type pair and said n-type pair each have an associated transconductance value of approximately g_m, said output stage including a compensation network which limits the
5 maximum amplifier bandwidth to avoid oscillation based on said transconductance value g_m.

18. The amplifier of claim 17, wherein said output stage includes a folded cascode gain stage and a rail-to-rail output stage,

said rail-to-rail output stage comprising first
5 and second complementary transistors connected to conduct respective currents to a common output node in response to first and second voltages applied to their respective control inputs,

said folded cascode gain stage arranged to
10 receive said differential output currents and provide said first and second voltages to said first and second complementary transistors,

said compensation network comprising a first capacitor connected between the control input of said first
15 complementary transistor and said common output node, and a second capacitor connected between the control input of said second complementary transistor and said common output node.

19. The amplifier of claim 13, wherein each of said switchable tail current sources comprise:

a bias voltage,

a current source transistor which conducts said
5 tail current when biased with a bias voltage, and

a switching transistor which couples said bias voltage to said current source in response to said first control signal.

20. A line-inversion LCD display driver, comprising:

a source driver suitable for switching one of a plurality of drive voltages to a column of LCD pixels in response to a digital code word, the transparency of each of said pixels varying over a predetermined pixel voltage range, each of said pixels receiving said selected drive voltage at its first terminal and alternately switched between first and second voltages at its second terminal, said source driver comprising a plurality of resistors connected in series and having accessible connection points at each end of said series string and at various resistor-resistor junctions along said series string, said series string producing at least some of said drive voltages when said connection points are connected to respective correction voltages, and

a grayscale reference generator circuit, comprising:

positive and negative supply rails,

a plurality of voltage sources providing respective correction voltages, half of said voltage sources providing correction voltages which are closer to said negative supply rail than said positive supply rail, and half of said voltage sources providing correction voltages which are closer to said positive supply rail than said negative supply rail,

a plurality of amplifiers interposed between said voltage sources and said resistor connection points, each of said amplifiers comprising:

first and second p-type transistors having respective control inputs, said first p-type transistor's control input connected to a respective one of said voltages sources providing a correction voltage which is closer to said negative supply rail than said positive supply rail,

35 a first switchable current source connected to supply tail current to said p-type transistors when enabled in response to a first control signal, said p-type transistors connected to provide a first differential output current when said tail current is supplied which 40 varies with a differential input signal applied to said p-type transistors' control inputs,

first and second n-type transistors having respective control inputs, said first n-type transistor's control input connected to a respective one of 45 said voltages sources providing a correction voltage which is closer to said positive supply rail than said negative supply rail,

a second switchable tail current source connected to supply tail current to said n-type transistors 50 when enabled in response to a second control signal, said n-type transistors connected to provide a second differential output current when said tail current is supplied which varies with a differential input signal applied to said n-type transistors' control inputs,

55 an output stage which receives said first and second differential output currents and is arranged to produce an output voltage at an output terminal which varies with said first and second differential output currents, said output terminal being said amplifier's 60 output, said output voltage coupled back to said second control inputs, and

a control circuit which provides said first and second control signals such that said first switchable current source is enabled and said second 65 switchable current source is disabled when the voltage at said first p-type transistor's control input is to be amplified by said amplifier, and said second switchable current source is enabled and said first switchable current

source is disabled when the voltage at said first n-type

70 transistor's control input is to be amplified by said amplifier.

each of said amplifier outputs connected to a respective one of resistor connection points,

said control circuit arranged to control

75 said first and second switchable current sources in synchronization with the switching of said pixels' second terminal such that the polarity of the voltages across said pixels is periodically reversed.